M.Tech (EMBEDDED SYATEMS)

Two Year (Four Semesters)

Scheme of Instruction and Syllabus

(Grading System)

(With effect from 2013-2014 admitted batch onwards)

Department of Electronics and Communication Engineering

Andhra University, Vishakapatnam-530003

2013

COURSE STRUCTURE

I SEMESTER

SUBJECT CODE	SUBJECT NAME	Credits	Periods/Week		Sessional Marks	University Exam Marks	Total
			Theory	Lab			
MTES-1	Digital Signal Processing	4	4	-	30	70	100
MTES-2	VLSI Design Techniques	4	4	-	30	70	100
MTES-3	Embedded Systems	4	4	-	30	70	100
MTES-4	Analog IC Design	4	4	-	30	70	100
MTES-5	Digital System Design	4	4	-	30	70	100
MTES-6	Elective-I	4	4	-	30	70	100
MTES-7	HDL Programming Lab	2	-	4	100	-	100
MTES-8	Seminar-1	2	-	2	100	-	100

Elective-I

a) EDA TOOLS
b) CPLD and FPGA Architecture and Applications
c) Digital Data Communications

II SEMESTER:

SUBJECT CODE	SUBJECT NAME	Credits	Periods/Week		Sessional Marks	University Exam Marks	Total
			Theory	Lab			
MTES-9	Embedded Computing Systems	4	4	-	30	70	100
MTES-10	Digital Design through HDL	4	4	-	30	70	100
MTES-11	DSP Processors and Architecture	4	4	-	30	70	100
MTES-12	Low Power VLSI Design	4	4	-	30	70	100
MTES-13	Microcontroller Applications	4	4	-	30	70	100
MTES-14	Elective-II	4	4	-	30	70	100
MTES-15	Embedded Systems Lab	2	-	4	100	-	100
MTES-16	Seminar-II	2	-	2	100	-	100

Elective-II

a) System Modeling & Simulation

b) Image Processing

c) Computer and Communication Networks

III SEMESTER:

Subject Code	*Subject title*	*Credits*	*Sessional Marks*	*University Exam Marks*	*Total*
MTES-17	Thesis (Part I)	15	50	50	100

Project work (PART-I) to be submitted before the end of 3rd Semester and it will be evaluated by a committee consisting of Chairman, Board of Studies, and Head of the Department and thesis guide.

IV SEMESTER:

Subject code	*Subject title*	*Credits*	*Sessional Marks*	*University Exam marks*	*Total*
MTES – 18	Thesis (Part II)	20	30	70	100

Thesis work is for a period of SIX months in Industry/Department. The students are required to submit their thesis two/three phases. Thesis is evaluated by a committee consisting of an external member from reputed institution, HOD, Chairman BOS and thesis Guide.

DIGITAL SIGNAL PROCESSING

Credits: 4

Subject Code: MTES-I **Max. Marks: 70**
I – Semester **Sessional: 30**

Common with M.Tech (Radar and Microwave Engineering (MTRM-I), M.Tech (VLSI (MTVL-I)), M.E. (Electronic Instrumentation)

UNIT -I

Advanced digital filter design techniques: Multiple band optimal FIR filters – design of filters with simultaneous constraints in time and frequency response, Optimization methods for designing IIR filters, comparison of optimum FIR filters and delay equalized elliptic filters.

UNIT -II

Multirate DSP : The basic sample rate alteration – time – domain characterization, frequency – domain characterization: Cascade equivalences, filters in sampling rate alteration systems, digital filter banks and their analysis and applications, multi level filter banks, estimations of spectra form finite – duration observation of signals.

UNIT -III

Linear prediction and optimum liner filters: forward and backward linear prediction, AR Lattice and ARMA lattice – ladder filters, Wieners filters for filtering on prediction.

UNIT -IV

DSP Algorithms: The Goertzel algorithm, the chirp – Z transform algorithm the Levinson – Durbin algorithms, the Schur algorithm, And other algorithms, computations of the DFT, concept of tunable digital filters.

UNIT - V

Signal Processing Hardware: Multipliers, dividers, different forms of FIR Hardware, multiplexing, DTTR, TDM to FDM translator, realization of frequency synthesizer, FIET hardware realization, different FT architectures, special FFT processors, convolvers, Lincoln laboratory FDP and the compatible computer configurations.

UNIT- VI

Applications of DSP: Speech: Models of speech production, speech analysis – synthesis system vocoder analyzers and synthesizers, linear prediction of speech. DTMF System.

Text Books:

1. Theory and applications of digital signal processing by Lawrence R. Rabiner and Bernard Gold, PHI
2. Digital Signal Processing. Principles, algorithms, and applications by Jhon G. Proakis and Dimitris G. Manolakis, PHI, 1997

Reference Books:

1. Digital Signal Processing, A Computer – Based approach, by Sanjit K. Mitra, Tata Mc Graw-hill, 1998.

VLSI DESIGN TECHNIQUES

Credits: 4

Subject Code: MTES -2 **Max. Marks: 70**
I-Semester **Sessionals: 30**

Common with M.Tech (VLSI (MTVL-2))

UNIT –I

INRODUCTION: Basic Principle of MOS Transistor, Introduction to Large Signal MOS Models (Long Channel) For Digital Design.

UNIT –II

The MOS Inverter, Layout and Simulation: Inverter principle, depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold. Noise Margins, and Dynamic behavior, Propagation Delay, Power Consumption. MOS Spice Model, Device Characterization, Circuit Characterization, Interconnects and Simulation. MOS Device Layout, Transistor Layout, Inverter Layout, CMOS Digital Circuits Layout & Simulation.

UNIT –III

Combinational MOS Logic Design: Static MOS design: Complementary MOS, Rationed Logic, Pass Transistor Logic, and complex logic circuits, Dynamic MOS Design, Dynamic Logic Families and Performances.

UNIT -IV

Sequential MOS Logic Design: Static Latches, Flip Flops and registers, Dynamic Latches and Registers, CMOS Schmitt trigger, Monostable Sequntial Circuits, Astable Circuits, Memory Design, ROM and RAM Cells Design

UNIT -V

Interconnect and Clock Distribution: Interconnect Delays, Cross Talks, Clock Distribution. Introduction to Low-power Design, Input and Output Interface circuits.

UNIT –VI

BICMOS Logic Circuits: Introduction, BJT Structure and Operation, Basic BICMOS Circuit behavior, Switching delay in BICMOS Logic Circuit, BICMOS Applications.

TEXT BOOKS:

1. Kang & Leblebigi CMOS Digital IC Circuit Analysis & Design" – Mc Graw Hill, 2003
2. Rabey, " Digital Integrated Circuits Design" Pearson Education, Second Edition, 2003

REFERENCE:

1. Weste and Eshraghian, " Principles of CMOS VLSI design" Addison – Wesley, 2002

EMBEDDED SYSTEMS

Credits: 4

Subject Code: MTES -3 **Max. Marks: 70**
I-Semester **Sessionals: 30**

UNIT -I

Introduction to Embedded Systems, Processor and Memory Organization:
Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit. Structural units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded system, allocation of memory to program segments and blocks and memory map of a system, DMA, interfacing processor, memories and Input Output Devices.

UNIT -II

Devices and Buses for Device Drivers and Networks: I/O devices, timer and counting devices, serial communication using the 'I2 C',' CAN and advanced I/O buses between the networked multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses. Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism.

UNIT -III

Programming Concepts and Embedded Programming in C and C++: Software programming in assembly language (ALP) and in high level language 'C','C' program elements: header and source files and preprocessor directives, program elements: macros and functions, data types ,data structures, modifiers , statements , loop and pointers, queues, stacks , lists and ordered lists, embedded programming in C++, embedded programming in java, 'C' program compiler and cross compiler , source code engineering tools for embedded C/C++,optimization of memory needs.

UNIT - IV

Program Modeling Concepts in Single and Multi-Processor Systems Software - Development Process: Modeling processes for software analysis before software implementation, programming models for event controlled or response time constrained real time programs, modeling of multi-processor systems.

UNIT -V

Hardware and Software Co Design – I: Embedded System project development, embedded System design and co-design issues in system development process, design cycle in the development phase for an Embedded System.

UNIT- VI

Hardware and Software Co Design – II: Use of target system or its Emulator and In-Circuit Emulator (ICE), use of Software tools for Development of an Embedded System, use of scopes and logic analyzers for System Hardware Tests.

TEXT BOOKS:

1. Raj Kamal, "Embedded systems: Architecture, programming and design", TMH, 2nd Edition, 2007.
2. Embedded System Design: A Unified Hardware/Software Introduction By Frank vahid/Tony Givargis john Wiley & sons

REFERENCES:

1. Arnold S Burger, "Embedded system Design", CMP books, 2010.
2. David Simon, "An embedded software primer", PEA, 2008.
3. Steve Heath, "Embedded systems Design", ELSEVIER, 2nd Edition 2005.

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ANALOG IC DESIGN

Credits: 4

Subject Code: MTES -4 **Max. Marks: 70**

I-Semester **Sessionals: 30**

Common with M.Tech (VLSI (MTVL-4))

UNIT -I

Integrated Circuit Devices and Modeling: MOS Transistors, Advanced MOS Modeling, Bipolar Junction Transistors, Device Model Summary, and SPICE modeling parameters.

UNIT -II

Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Source Follower, Common Gate Amplifier, High Output Impedance Current Mirrors and Bipolar Gain Stages, Frequency Response.

UNIT -III

Operational Amplifier Design and Compensation: Two Stage CMOS Operational Amplifier, Feedback and Operational Amplifier Compensation, Comparator, Charge Injection Error, Latched Comparator and Bi CMOS Comparators.

UNIT -IV

Advanced Current Mirrors and Operational Amplifiers: Advanced Current Mirror, Folded – Cascade Operational Amplifier, Current Mirror Operational Amplifier, Fully Differential Operational Amplifier. Common Mode Feedback Circuits, Current Feedback Operational Amplifier.

UNIT –V

Sample and Hold& Switched Capacitor Circuits: MOS Sample – and - Hold Basics, CMOS sample and Hold Circuits, Bipolar and Bi CMOS sample and holds. Basic Operation and Analysis, First – Order and Biquad Filter, Charge Injection, Switched Capacitor gain Circuits, Correlated Double - Sampling Techniques, Other Switched Capacitor Circuits.

UNIT -VI

Data Converters: Ideal D/A & A/D Converters, Quantization Noise, Performance Limitations, Nyquist Rate D/A Converters: Decoder Based Converters, Binary Scaled Converters, Hybrid Converters. Nyquist Rate A/D Converters: Integrating, Successive Approximation, Cyclic, Flash Type, Two Step, Interpolating, Folding A/D Converters and Pipelined A/D Converters. Over Sampling with and Without Noise Shaping, Digital Decimation Filter, High Order Modulators, Band Pass Oversampling Converter.

TEXT BOOK:

1. D.A.JOHN & KEN MARTIN: Analog Integrated Circuit Design. John Wiley, Reprint 2008.

REFERENCE BOOKS:

1. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

DIGITAL SYSTEM DESIGN

Credits: 4

Subject Code: MTES -4 **Max. Marks: 70**
I-Semester **Sessionals: 30**

Common with M.Tech (VLSI (MTVL-5))

UNIT –I

Design of Digital Systems: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT –II

Sequential Circuit Design: Design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT –III

Fault Modeling: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults. **Test Generation:** Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT -IV

Test Pattern Generation: D – Algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT -V

Fault Diagnosis in Sequential Circuits: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT –VI

Programming Logic Arrays and Asynchronous Sequential Machine: Design using PLA's, PLA minimization and PLA folding. Fault models, Test generation and Testable PLA design. Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXT BOOKS:

1. Zvi Kohavi, "Switching and Finite Automata Theory", TMH, 2nd Edition, 2005,
2. N. N. Biswas, "Logic Design Theory", PHI, 2009.
3.Norman Balabanian, Bradley Carlson, "Digital Logic Design Principles" Wiley Student Edition, 2007, Reprint

REFERENCE BOOKS:

1. M. Abramovici, Melnin Breuer, Arthur Friedman–"Digital System Testing and Testable Design", Jaico Publications, 2008, Reprint Edition
2. Charles H. Roth Jr. – "Fundamentals of Logic Design", Cengage learning, 2004 6th Edition.
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition, 1993.

ELECTIVE-I

ELECTRONIC DESIGN AUTOMATION TOOLS

Credits: 4

Subject Code: MTES -6(a) **Max. Marks: 70**

I-Semester **Sessionals: 30**

Common with M.Tech (VLSI (MTVL-6 (C))

UNIT -I

Important Concepts in Verilog: Basics of Verilog Language, Operators, Hierarchy, Procedures and Assignments, Timing Controls and Delay, Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, Other Verilog Features.

UNIT -II

Synthesis and Simulation Using HDLS: Verilog and Logic Synthesis, VHDL and Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis .Simulation-Types of Simulation, Logic Systems, Working Of Logic Simulation, Cell Models, Delay Models State Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation. CAD Tools for Synthesis and Simulation Modalism and Leonardo Spectrum (Exemplar).

UNIT -III

Tools for Circuit Design and Simulation Using PSPICE: Pspice Models For Transistors, A/D & D/A Sample and Hold Circuits Etc, and Digital System Building Blocks, Design and Analysis Of Analog and Digital Circuits Using PSPICE.

UNIT -IV

An Over View of Mixed Signal VLSI Design: Fundamentals Of Analog and Digital Simulation, Mixed Signal Simulator Configurations, understanding Modeling, Integration to CAD Environments.Eg.A/D, D/A Converters, Up And Down Converters, Comparators Etc.

UNIT -V

Tools for PCB Design and Layout

An Overview Of High Speed PCB Design, Design Entry, Simulation and Layout Tools for PCB, introduction to Orcad PCB Design Tools.

TEXT BOOKS:

1. J.Bhasker, A Verilog Primer, BSP, 2003 3rd Edition.
2. J.Bhasker, A Verilog HDL Synthesis BSP, 2003, 2nd Edition.
3. M.H.RASHID: SPICE FOR Circuits and Electronics Using PSPICE (2/E) (1992) Prentice Hall.

REFERENCES:

1. ORCAD: Technical Reference Manual, Orcad, USA.
2. SABER: Technical Reference Manual, Analogy Nic, USA.
3. M.J.S.SMITH: Application-Specific Integrated Circuits (1997).
Addison Wesley
4. J.Bhasker, A VHDL Synthesis Primer, BSP, 2003, 3rd Edition.

ELECTIVE-I

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

Credits: 4

Subject Code: MTES -6(b) **Max. Marks: 70**

I-Semester **Sessionals: 30**

Common with M.Tech (VLSI (MTVL -11)

UNIT -I

Programmable Logic Devices: ROM, PLA, PAL, PLD, PGA – Features, programming, applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT –II

CPLDs: programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT –III

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs , Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT- 1,2,3 and their speed performance.

UNIT -IV

Finite State Machines (FSM): Top down Design – State Transition Table, state assignments for FPGAs, Realization of state machine charts with a PAL. Alternative realization for state machine chart using microprogramming. Linked state machines. Encoded state machine. Architectures centered around non-registered PLDs, Design of state machines centered around shift registers, One Hot machine, Petrinets for state machine – Basic concepts and properties, Finite state machine – case study.

UNIT –V

Design Methods and System Level Design: One – Hot Design method, Use of ASMs in One – Hot Design Method, Applications of One-Hot Design Method, Extended Petri-nets for parallel controllers, Meeta stability, Synchronization, Complex design using shift registers. Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs.

UNIT –VI

Case studies: Design consideration using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology- S.Trimberger, Edr.1994, Kluwer Academic Publications,
2. Engineering Digital Design –RICHARD F.TINDER,2nd Edition, Academic press,
3. Fundamentals of logic design-Charles H. Roth, 4th Edition jaico publishing House.

REFERENCE:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S.Mourad,1994, Prentice hall
2. Field programmable Gate Array, S.Brown, R.J.Francis, J.Rose, Z.G.Vranesic, 2007, BSP

ELECTIVE-I

DIGITAL DATA COMMUNICATIONS

Credits: 4

Subject Code: MTES -6(c) **Max. Marks: 70**

I-Semester **Sessionals: 30**

UNIT –I

Digital Modulation Techniques: FSK, MSK, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK Methods, Bandwidth efficiency, Carrier recovery, Clock recovery.

UNIT- II

Data Communication Methods and Protocols: Data Communication Circuit, point-to-point, Multi-point configurations and Topologies, transmission modes, 2-wire and 4-wire operations, Codes, Error detection methods, Error correction methods, Character synchronization. Asynchronous protocols, Synchronous protocols, Bisync Protocol, SDLC, HDLC-Frame format, Flow control and error control.

UNIT- III

Switching Techniques: Circuit Switching, Message Switching and Packet Switching principles, Virtual circuit and datagram techniques, X.25 and frame relay.

UNIT- IV

Line Protocols and Congestion Control: Line protocols: Basic mode, Half-duplex point-to-point protocol, Half- Duplex Multi-Point Protocol, Full-Duplex Protocols, Polling, Roll Call and Hub Polling, Traffic management, Congestion control in packet switching networks and Frame relay.

UNIT- V

Digital Multiplexing: TDM, T1 carrier system, CCITT-TDM carrier system, CODEC chips, Digital hierarchy, Line Encoding, Frame Synchronization. Multiplexers, Statistical multiplexer, Concentrator, front-end communication processor, Digital PBX, long haul communication with FDM, Hybrid data.

UNIT- VI

Optical Communication: Basic Optical Network Topologies and their performances, SONET/SDH – Transmission formats and Speeds, Optical interfaces, SONET/SDH rings and networks.

TEXT BOOKS:

1. W. TOMASI: Advanced Electronic Communications Systems, PHI, 6th Edition 2004.
2. William Stallings “Data and Computer Communications” , 7/e, PEI.
3. B.Gerd Keiser, “Optical Communications”, PHI 4th Edition, 2008.

REFERENCES:

1. T. HOUSELY: Data Communications and Teleprocessing Systems, PHI. 2nd Edition, 1987
2. B.A.Forouzon, “Data and Computer Networking Communications”, 3rd TMH, 2010.

HDL PROGRAMMING LAB

Credits: 2

Subject Code: MTES -7 **Max. Marks: 50**

I-Semester **Sessionals: 50**

Common with M.Tech (VLSI (MTVL -7))

1. Basic Gates
2. Adders
3. Subtractors
4. Full Adder using Two Half Adders
5. Decoders
6. 4 Bit Binary Adders
7. Multiplexers
8. Encoders
9. Demutiplexers
10. Comparators
11. Flip Flops
12. Counters
13. Shift Registers
14. Mealy & Moore Machine for sequence detector
15. Implementation of ALU
16. Implementation of clock generator.

EMBEDDED COMPUTING SYSTEMS

Credits: 4
Subject Code: MTES-9 **Max Marks: 70**
II-SEMESTER **Sessionals: 30**

UNIT-I:
Programming on Linux Platform
System calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root file System, Busy Box.

UNIT-II:
Operating System Overview: Processes, Tasks, Threads, Multi Threading, Semaphore, Message Queue.

UNIT-III:
Introduction to Software Development Tools:
GNU GCC, make, gdb, static and dynamic linking, C Libraries, Compiler Options, Code Optimization Switches, lint, code profiling tools.

UNIT IV:
Interfacing Modules:
Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, open CV for machine vision, Audio signal processing.

UNIT V:
Networking Basics:
Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SBH, firewall, network security.

UNIT VI:
IA32 Instruction Set: Application Binary Interface, Exception and Interrupt Handling, Interrupt Latency, Assemblers, Assembler Directives, Macros, Simulation and debugging Tools.

TEXT BOOKS:
1. Modern Embedded Computing-Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kauffmann, 2012.
2. Linux Application Development-Michael K.Johnson, Erik W.Troan, Adission Wesley, 1998.

REFERENCE BOOKS:

1. Operating System Concepts by Abraham Silberschatz, Peter B.Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J.Bach Prentice-Hall
3. UNIX Network programming by W.Richard Stevens
4. Assembly Language for X86 Processors by Kip R.Irvine

DIGITAL DESIGN THROUGH HDL

Credits: 4

Subject Code: MTES-10 **Max Marks: 70**

II-SEMESTER **Sessionals: 30**

UNIT-I

The VHDL Design and combinational and Sequential Logic Design (Using VHDL)

Structural design elements, data flow design elements, behavioral design elements, and time dimension and simulation synthesis. Decoders, encoders, three state devices, multiplexers and Demutiplexers, Code Converters, EX-OR gates and parity circuits, comparators, adders & Sub tractors, ALUs, Combinational multipliers. VHDL codes for the above ICs Barrel shifter, comparators, floating point encoder, dual priority encoder, Latches and flip-flops, PLDs, counters, shift register and their VHDL models, synchronous design methodology, impediments to synchronous design.

UNIT-II

Introduction to Verilog, Language Constructs and Conventions

Introduction ,Keywords, Identifiers, Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches. White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT-III

Gate Level Modeling

Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits.

UNIT-IV

Behavioral Modeling

Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow, i*f* and i*f*-else constructs, assign-design construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT-V

Modeling at Data Flow Level and Switch Level Modeling

Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators. Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

UNIT-VI

System Tasks, Functions, and Compiler Directives and Digital Design with SM Charts
Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises. Introduction, Function, Tasks, User- Defined Primitives (UDP), FSM Design (Moore and Mealy Machines). State Machine Charts, Derivation of SM Charts, Realization of SM Charts.

Text Books

1. John F.Wakerly, "Digital Design Principles &Practices", PHI/Pearson Education, 3rd Ed, 2005
2. T.R.Padmanabhan and B.Bala Tripura Sundari, "Design through Verilog HDL", WSE, IEEE Press, 2004.

References:

1. J.Bhasker, "VHDL Primer", PHI, 3rd Edition, 1999. Michael D.Ciletti, "Advanced Digital Design with Verilog HDL", PHI, 2nd Edition, 2005.
2. Samir Palnitkar, "Verilog HDL", 2dn Edition, 2003.
3. J.Bhasker, "A Verilog HDL primer", SG Press, 2nd edition, 1997.

DSP PROCESSORS AND ARCHITECTURE

Credits: 4

Subject Code: MTES-11 **Max Marks: 70**

II-SEMESTER **Sessionals: 30**

Common with M.Tech (VLSI (MTVL -14(c)))

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESSING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES AND EXECUTION

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing. Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT IV

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS AND FFT ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing. An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing- Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features- Lapsley et al.S.Chand & Co, 2000.

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and Applications-B. Venkata Ramani and M. Bhaskar, TMH,2004.
2. Digital Signal Processing-Jonatham Stein, John Wiley, 2005.

LOW POWER VLSI DESIGN

Subject Code: METS-12 **Credits: 4**
II- Semester **Max. Marks: 70**
Sessionals: 30

Common with M.Tech (VLSI (MTVL-12))

UNIT I
LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II
MOS/Bi-CMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process. Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT III
DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT IV
CMOS AND BI-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance evaluation.

UNIT V
LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits. ESD-free BiCMOS, Digital circuit operation and comparative Evaluation.

UNIT VI
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS:
1. Low power by Yeo Rofail/Gohl (3 Authors), "CMOS/Bi CMOS ULSI Low Voltage", - Pearson Education Asia 1st Indian reprint, 2002.

REFERENCES:
1. Digital Integrated circuits, J.Rabaey, "PH. N.J 1996.
2. CMOS Digital ICs Sung-mokang and yusuf leblebici, 3rd edition TMH 2003(Chapter 11)
3. VLSI DSP Systems, Parhi, John Wiley & sons, 2003(Chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

MICROCONTROLLER AND APPLICATIONS

Credits: 4
Subject Code: MTES-13 **Max Marks: 70**
II-SEMESTER **Sessionals: 30**

UNIT-I

Overview of Architecture and microcontroller Resources

Architecture of a microcontroller – Microcontroller resources – Resources in advanced and next generation microcontrollers – 8051 microcontroller – Internal and External memories – Counters and Timers – Synchronous serial-cum-asynchronous serial communication - Interrupts.

UNIT-II

8051 Family Microcontrollers Instruction Set

Basic assembly language programming – Data transfer instructions – Data and Bit manipulation instructions – Arithmetic instructions – Instructions for Logical operations on the 'Bytes' among the Registers, Internal RAM, and SFRs – Program flow control instructions – Interrupt control flow.

UNIT-III

Real Time Control and Timers

Interrupt handling structure of an MCU – Interrupt Latency and Interrupt deadline – Multiple sources of the interrupts – Non-maskable interrupt sources – Enabling or Disabling of the sources – Polling to determine the Interrupt source and assignment of the priorities among them – Interrupt structure in Intel 8051.Programmable Timers in the MCUs – Free running counter and real time control – Interrupt interval and density constraints.

UNIT-IV

Systems Design

Digital and Analog Interfacing Methods, Switch, Keypad and Keyboard interfacings – LED and Array of LEDs – Display Systems and its interfaces – Printer interfaces – Programmable instruments interface using IEEE 488 Bus – Interfacing with the Flash Memory – Interfaces – Interfacing to High Power Devices – Analog input interfacing – Analog output interfacing.

UNIT V

Real Time Operating System and Arm 32 Bit MCUs

Introduction to 16/32 Bit processors – ARM architecture and organization – ARM / Thumb programming model – ARM / Thumb instruction set – Development tools. Real Time operating system – RTOS of Keil (RTX51) – Use of RTOS in Design – Software development tools for Microcontrollers.

UNIT VI

Microcontroller Based Industrial Applications

Optical motor shaft encoders – Industrial control – Industrial process control system – Prototype MCU based Measuring instruments – Robotics and embedded control – Digital Signal Processing and Digital Filters.

TEXT BOOKS:

1. Raj Kamal, "Microcontrollers Architecture, Programming Interfacing and System Design", Pearson Education, 2005, 2nd Edition
2. Mazidi and Mazidi, "The 8051 Microcontroller and Embedded Systems", PHI, 2000, 4th impression.

REFERENCE BOOKS:

1. A.V. Deshmuk, "Microcontrollers (Theory & Applications)"–, TMH, 6th Reprint, 2007.
2. John B. Peatman, "Design with PIC Microcontrollers", Pearson Education, 2005, 2nd Edition.

ELECTIVE-II

SYSTEM MODELLING & SIMULATION

Credits: 4

Subject Code: MTES-14(a) **Max Marks: 70**

II-SEMESTER **Sessionals: 30**

Common with M.Tech (VLSI (MTVL-10))

UNIT-I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT-II

SIMULATION SOFTWARE:

Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT-III

BUILDING SIMULATION MODELS AND MODELING TIME DRIVEN SYSTEMS

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility. Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT-IV

EXOGENOUS SIGNALS AND EVENTS

Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation. Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT-V

EVENT DRIVEN MODELS

Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

UNIT-VI

SYSTEM OPTIMIZATION

System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodogy.

TEXT BOOKS:

1. System Modeling & Simulation, An Introduction - Frank L. Severance, John Wiley & Sons 2001.
2. Simulation Modeling and Analysis- Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFERENCE BOOKS:

1. Systems Simulation- Geoffery Gordon, PHI, 1978.

ELECTIVE-II

DIGITAL IMAGE PROCESSING

Subject Code: METS-14(b) **Credits: 4**
II- Semester **Max. Marks: 70**
Sessionals: 30

Common with M.Tech (RADAR AND MICROWAVE ENGINEERING (MTRM-14(c)))

UNIT I

Digital Image Fundamentals: An Image model- sampling & quantization- basic relation between pixels: imaging geometry. Image Transforms: properties of 2-D Fourier Transform, FFT algorithm and other separable image transforms, Walsh transforms, Hadamard, Cosine, Haar, Slant transforms, RL transforms and their properties.

UNIT II

Image Enhancement and Restoration:

Spatial domain methods, Frequency domain methods, Histogram modification technique, Neighborhood averaging median filtering, Low pass filtering, Averaging of multiple images, Image Sharpening by differentiations, High Pass Filtering, Degradation model for continuous functions, Discrete formulation, Diagonalization of circulate and block – Circulant matrices, effects of Diagonalization, Constrained and unconstrained restoration inverse filtering, Wiener filter, Constraint least square restoration.

UNIT III

Image Encoding: Objective and subjective Fidelity Criteria, the encoding process, the Mapping, the Quantizer and the Coder, Contour Encoding, Run length Encoding, Image Encoding relative to a Fidelity Criterion, Differential Pulse Code Modulation, Transform Encoding.

UNIT IV

Image Compression: Fundamentals, Image Compression Models, error free compression, Lossy compressions, Image Compression Standards.

UNIT V

Image Segmentation: The Detection of discontinuities, point line and Edge detection, Gradient operators, combined detection, thresholding.

UNIT VI

Image Representation: Representation schemes, chain codes, polygon Approximation, Boundary Descriptors, Simple descriptors, shape number, Fourier Descriptors. Image construction from projections: Random transforms, Convolution/ filter back Projection

TEXT BOOKS:

1. Gonzalez RC & Woods RE, Digital Image Processing Addison Wesley Publishing Company.
2. Jain AK, Fundamentals of Digital Image Processing, PHI.

REFERENCES:

1. Rosefeld & Kak AC, Digital picture processing Academic Press INC.

ELECTIVE-II

COMPUTER AND COMMUNICATION NETWORKS

Credits: 4
Subject Code: METS-14(b) **Max. Marks: 70**
II- Semester **Sessionals: 30**
Common with M.Tech (RADAR AND MICROWAVE ENGINEERING (MTRM-12(b)))

UNIT-I
Introduction to Computer Networks, OSI Reference Model: A Layered Approach, Intro to TCP/IP Protocol Suite.

UNIT-II
Transmission Media and Digital Signaling, Analog vs. Digital Transmission, Nyquist and Shannon Limits, Digital or Analog Data to Digital Signals.

UNIT-III
Wireless Communication, Advances in cellular, personal communications systems (PCS), global system for mobile communications (GSM), wireless LANs - applications, satellites, and fixed wireless networks.

UNIT-IV
Error Detection and CRC Polynomial Codes. Data Link Control, Stop & Wait, Sliding Window ARQ, Go-back-N, Selective Reject.

UNIT-V
Data Link Layer Protocols and Multiplexing, HDLC, LAP-B, ARPANET DLC, Frequency and Time Division Multiplexing.

UNIT-VI
Circuit Switching and Packet Switching, Digital Switching Concepts, Packet Switching principles, Virtual Circuits and Datagrams, X.25, Frame and Cell Relay, ATM.

TEXT BOOKS:

1. William Stallings, "Wireless Communications and Networks", Prentice Hall, 2004
2. Stallings, William Data and Computer Communications, 8th Edition Prentice Hall, 2007,

REFERENCE BOOKS:

1. T.S. Rappaport, "Wireless Communications: Principles & Practice", Second Edition, Prentice Hall, 2002.
2. J R. Prasad, W. Mohr, and W. Konhauser (Editors), "Third Generation Mobile Communication Systems", Artech House Publishers, 2000.
3. W.C.Y. Lee, "Mobile Communication Engineering, Theory and Applications", Second Edition, McGraw-Hill, 1998.

EMBEDDED SYSTEM LAB

Credits: 2
Subject Code: MTES-15 **Max. Marks: 50**
II- Semester **Sessionals: 50**

Note: Minimum of 6 programs from Part-I and 6 programs from Part-II are to be conducted.

PART-I:

The following programs are to be implemented on ARM processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly program to configure and control General Purpose Input/output (GPIO) Port pins.
3. Write an Assembly Programs to read digital values from external peripherals and execute them with the Target Board.
4. Program for reading and writing of a file.
5. Program to demonstrate Time delay program using built in Timer/ Counter feature on IDE environment.
6. Program to demonstrate a simple interrupt handler and setting up a timer.
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment.
10. Program to displaying a message in a 2 line x 16 characters LCD display and verify the result in debug terminal.

PART-II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE environment using ARM Tool chain and library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task.
3. Write an application that Demonstrate the interruptible ISRs (Require timer to have higher Priority than external interrupt button)
4. a) Write an application to Test message queues and memory blocks.
   b) Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings.
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mail box by one task and reading the message from mail box from another task.
9. Sending message to PC through serial port by three different tasks on priority Bases.
10. Basic Audio Processing on IDE environment.

III SEMESTER:

Subject Code	*Subject title*	*Credits*	*Sessional Marks*	*University Exam Marks*	*Total*
MTES-17	Thesis (Part I)	15	50	50	100

Project work to be submitted before the end of 3rd Semester and it will be evaluated by a committee consisting of Chairman, Board of Studies, Head of the Department and thesis guide in the AUCE(A) and in the Affiliated Colleges Thesis (Part I) will be evaluated by concerned Head of the Department and thesis guide of their respective colleges.

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IV Semester:

Subject code	*Subject title*	*Credits*	*Sessional Marks*	*University Exam marks*	*Total*
MTES – 18	Thesis (Part II)	20	30	70	100

Thesis work is for a period of SIX months in Industry/Department. The students are required to submit their thesis in two/three phases. Thesis is evaluated by a committee consisting of an external member from reputed institution, HOD/ Chairman BOS and thesis Guide.